UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,677	10/14/2005	Tae Ha Ryoo	11005-028-999	7258

20583 7590 01/25/2007

JONES DAY
222 EAST 41ST ST
NEW YORK, NY 10017

EXAMINER	
LAO, LUN S	
ART UNIT	**PAPER NUMBER**
2615	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/527,677	RYOO ET AL.	
	Examiner	Art Unit	
	Lun-See Lao	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This action is response to the application filed on 10-14-2005. Claims 1-9 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walburger (US PAT 6,597,240) in view of Hasegawa (US PAT. 6,169,449).

Consider claim 1 Walburger teaches that a circuit for eliminating pop noise including a power PMOS transistor (see fig.3 (302b) having a source to which a first power supply voltage (V_D) is applied and a drain connected to an output terminal, a power NMOS (302a) transistor having a drain connected to the output terminal and a source to which a second voltage (ground V0) is applied, a gate controller (308a, 308b) that controls a gate of the power PMOS transistor (302b) and a gate of the power NMOS transistor (302a), and an output-terminal filter (110) having an inductor (318) and a capacitor (110), the circuit comprising:

a first switch (306b), which is connected between the first power supply

voltage (V_D) and the gate of the power PMOS transistor (302b);

a second switch (306a), which is connected between the second voltage (ground V0) and the gate of the power NMOS transistor (302a); and

a switch controller (308a, 308b), which senses the first power supply voltage (V_D) and the second voltage (ground, V0) and generates a first control signal for controlling the first switch (306b) and a second control signal for controlling the second switch (306a) (see col. 3 line 54-col. 4 line30),

wherein the switch controller (308a, 308b) turns on the first switch (306b) and the second switch (306a) until the first power supply voltage (V_D) and the second voltage (ground V0) reach respective threshold voltages (Vref) and turns off the first switch (306b) and the second switch (306a) after the first power supply voltage and the second voltage (ground V0) reach respective threshold voltages (see fig.4 and col. 4 line 31-col. 5 line 22); but the second voltage connected between the second switch of Walburger is not a second power supply voltage.

However, Hasegawa teaches a switch controller (see fig.4 (322)), which senses the first power supply voltage (VDD1) and the second power supply voltage (VDD2) and generates a first control signal for controlling the first switch (22) and a second control signal for controlling the second switch (23'),

wherein the switch controller (322) turns on the first switch (22) and the second switch until (23') the first power supply voltage (VDD1) and the second power supply voltage (VDD2) reach respective threshold voltages and turns off the first switch and the second switch (22,23') after the first power supply voltage and the

second power supply voltage (VDD1, VDD2) reach respective threshold voltages (see col. 6 line 17-col. 7 line 67) .

Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hasegawa into Walburger to reduce the electric power consumption by decrease the electric current caused to flow through the transistor on the low power transmission within a predetermined output range.

Consider claim 9 it is a method claim corresponding to a circuit claim 1. See previous circuit claim 1 rejection.

Consider claims 2-3 Walburger teaches that the first switch (see fig.3, (306b)) comprises:

a PNP-type bipolar transistor (see fig.3, (304b), which has an emitter to which the first power supply voltage (V_D) is applied and a base to which the first control signal is applied; and a diode (320b), which has one terminal connected to a collector of the PNP (304b) type bipolar transistor and the other terminal connected to the gate of the power PMOS (302b) transistor (see col. 3 line 54-col. 4 line30); and

the circuit of the second switch (see fig.3, (306a) comprises:

an NPN-type bipolar transistor (304a), which has an emitter to which the second voltage (ground V0) is applied and a base to which the second control signal is applied; and a diode (320a), which has one terminal connected to a collector of the NPN-type bipolar transistor (304a) and the other terminal connected to the gate of the power NMOS (302b) transistor (see col. 3 line 54-col. 4 line 30 and see the discussion above claim 1).

Consider claims 4-5 Walburger teaches that the first switch (see fig.3, (306b)) comprises a PMOS transistor (302b) having a source to which the first power supply voltage (V_D) is applied, a gate to which the first control signal is applied, and a drain connected to the gate of the power PMOS transistor (302b and see col. 3 line 54-col. 4 line30); and the circuit of the second switch (see fig.3, (306a)) comprises an NMOS transistor (302a) having a source to which the second voltage (ground V0) is applied, a gate to which the second control signal is applied, and a drain connected to the gate of the power NMOS transistor (302a and see col. 3 line 54-col. 4 line 30 and see the discussion above claim 1).

Consider claim 6 Hasegawa teaches that the circuit of the switch controller (see fig. 4 (322)) comprises:

a first control portion (22), which senses the first power supply voltage (VDD1) and generates the first control signal; and

a second control portion (23'), which senses the second power supply voltage (VDD2) and generates the second control signal (see col. 6 line 17-col. 7 line 67).

Allowable Subject Matter

4. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Padi (US PAT 5,162,752) is cited to show other related circuit and method for eliminating pop noise in digital audio amplifier using dual power supply.

6. Any response to this action should be mailed to:

Mail Stop ____(explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:
(571) 273-8300

Hand-delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501 The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao,Lun-See L.S.
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501
Date 01-12-2007

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600